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L24	L23 and l21	0	L24
L23	717/127,128,130,131,132,154.ccls.	830	L23
L22	L21 and pipelin$ and execut$	1	L22
L21	(conjugat$ near4 process$) and (conjugat$ near4 (map$ or match$))	57	L21
L20	(conjugat$ near4 processor) and (conjugat$ near4 mapp$)	0	L20
L19	(conjugat$ near4 processor) and (conjugat$ near4 mapp$)	0	L19
DB=TDBD; PLUR=YES; OP=ADJ			
L18	(h-flow or h flow or conjugate) and pipeline and map$ and entr$ and trigger$ and execut$	0	L18
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L13	(h-flow or h flow or conjugate) and pipeline and map$ and entr$ and trigger$ and execut$	30	L13

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L12	19 and map$ and entr$ and trigger$	8	L12
L11	19 and conjugat$	0	L11
L10	L9 and (trigger$ near4 satisf$)	0	L10
L9	(pipeline$ near5 execut$ near5 modif$)	64	L9
L8	(conjugat$) near5 pipeline$ near5 (modif$ or updat$ or chang$) and execut$	0	L8
L7	L6 and execut$	0	L7
L6	11 and pipeline near5 (chang$ or modif$ or alter$)	6	L6
L5	11 and (trigger$ near5 satis$ neat6 execut$)	0	L5
L4	11 and ((h-flow) or (conjugate flow)) near5 (code$ or program$)	0	L4
L3	(h-flow or h flow or (conjugat$ near4 flow)) and (pipeline$ near5 execut$)	3	L3
L2	(h-flow or h flow or (conjugat$ near4 flow)) near5 pipeline$	3	L2
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1 Synthesis of pipelined instruction set processors   ■
Richard J. Cloutier, Donald E. Thomas
July 1993 **Proceedings of the 30th international conference on Design automation**

Full text available: 📄 pdf(796.47 KB) Additional Information: full citation, references, citings, index terms

2 Automatic Verification of In-Order Execution In Microprocessors with Fragmented   ■
Pipelines and Multicycle Functional Units
P. Mishra, N. Dutt, A. Nicolau, H. Tomiyama
March 2002 **Proceedings of the conference on Design, automation and test in Europe**

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As embedded systems continue to face increasingly higherperformance requirements,
deeply pipelined processor ar-chitecturesare being employed to meet desired system per-
formance.System architects critically need modeling tech-niquesthat allow exploration,
evaluation, customizationand validation of different processor pipeline configurations,tuned
for a specific application domain. We propose a novelFinite State Machine (FSM) based
modeling of pipelinedprocessors and define a set of properties th ...

3 Instruction issue logic for high-performance, interruptable pipelined processors   ■
G. S. Sohi, S. Vajapeyam
June 1987 **Proceedings of the 14th annual international symposium on Computer architecture**

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The performance of pipelined processors is severely limited by data dependencies. In order
to achieve high performance, a mechanism to alleviate the effects of data dependencies
must exist. If a pipelined CPU with multiple functional units is to be used in the presence of
a virtual memory hierarchy, a mechanism must also exist for determining the state of the
machine precisely. In this paper, we combine the issues of dependency-resolution and
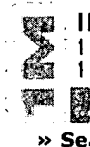preciseness of state. We present a design for in ...

4   ■
Code size reduction technique and implementation for software-pipelined DSP

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